Intel® High Definition Audio Specification Document Change Notification

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Document Revision: Intel® High Definition Audio 1.0

This document discloses changes to the Intel® High Definition Audio Specification and all information contained herein is provided under the terms of the "AZALIA" SPECIFICATION DEVELOPMENT AGREEMENT" also known as Intel® High Definition Audio Specification Developer Agreement, and all the terms of such agreement, including the confidentiality provisions, shall apply to this disclosure.

Title: Clarification of CORB & RIRB Size Read/Write requirement

Brief description of the functional changes:

The definition in the HD Audio specification requires that the CORBSIZE and RIRBSIZE fields of the CORB & RIRB size registers be Read/Write, even though the controller is only required to support one size. When only one size is implemented, then the capability to write the size register is not possible.

Current Definitions:

3.3.24 Offset 4Eh: CORBSIZE - CORB Size

Length: 1 byte

Table 1. CORB Size

Bit	Туре	Reset	Description				
			CORB Size Capability (CORBSZCAP): A bit mask indicating the sizes of the CORB supported by the controller.				
				Bits [7:4]	CORB Size		
				0001	8 B = 2 entries		
7:4	RO	Imp.Dep		0010	64 B = 16 entries		
				0100	1024 B = 256 Entries		
				1000	Reserved		
					r example, if the controller s yould have a value of 0101b	• •	
3:2	RsvdP	0	Reserved				

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Bit	Туре	Reset	Description			
	RW	Imp.Dep	CORB Size (CORBSIZE): The setting of the register determines when the address counter in the DMA controller will wrap around.			
1:0				Bits [1:0]	CORB Size	
			0	00	8 B = 2 entries	
				01	64 B = 16 entries	
				10	1 KB = 256 entries	
				11	Reserved	

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3.3.31 Offset 5Eh: RIRBSIZE - RIRB Size

Length: 1 byte

Table 2. RIRB Size

Bit	Туре	Reset	Description				
		Imp.Dep	RIRB Size Capability (RIRBSZCAP):				
			A bit mask identifying the possible sizes of the RIRB.				
				Bits [7:4]	RIRB Size		
				0001	16 B = 2 entries		
7:4	RO			0010	128 B = 16 entries		
				0100	2048 B = 256 Entries		
				1000	Reserved		
			This implemented as a bit mask; for example, if the controller supported two entries and 256 entries, this register would be Read Only 0101b.				
3:2	RsvdP	0	Reserved				
	RW	Imp.Dep	RIRB Size (RIRBSIZE): The setting of the register determines when the address counter in the DMA controller will wrap around.				
				Bits [1:0]	RIRB Size		
				00	16 B = 2 entries		
1:0				01	128 B = 16 entries		
				10	2 KB = 256 entries		
				11	Reserved		
			This value must not be changed when the RIRB DMA engine is enabled.				

New Definition:

3.3.24 Offset 4Eh: CORBSIZE - CORB Size

Length: 1 byte

Table 3. CORB Size

		CORB supported by the co	ORBSZCAP): A bit mask indicating tontroller.	he sizes of the
		Dita [7, 4]		
		Bits [7:4]	CORB Size]
		0001	8 B = 2 entries	
		0010	64 B = 16 entries	
RO	Imp.Dep	0100	1024 B = 256 Entries	
		1000	Reserved	
There is no requirement to support more than one CORB Si RsvdP 0 Reserved CORB Size (CORBSIZE): The setting of the register determination of the register determination.				
RW or RO if only one size supported	Imp.Dep		CORB Size	1
		00	8 B = 2 entries	
		01	64 B = 16 entries	
		10	1 KB = 256 entries	
		11	Reserved	
	RsvdP RW or RO if only one size	RsvdP 0 RW or RO if only one size	This is implemented as a bentries and 256 entries, thi There is no requirement to RsvdP 0 Reserved CORB Size (CORBSIZE): address counter in the DM Bits [1:0] 00 01 10 11	This is implemented as a bit mask; for example, if the controller entries and 256 entries, this register would have a value of 0101 There is no requirement to support more than one CORB Size. RsvdP 0 Reserved CORB Size (CORBSIZE): The setting of the register determine address counter in the DMA controller will wrap around. Bits [1:0] CORB Size 00 8 B = 2 entries 01 64 B = 16 entries 10 1 KB = 256 entries

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3.3.31 Offset 5Eh: RIRBSIZE - RIRB Size

Length: 1 byte

Table 4. RIRB Size

Bit	Туре	Reset	Description				
			RIRB Size Capability (RIRBSZCAP):				
			A bit mask id	mask identifying the possible sizes of the RIRB.			
				Bits [7:4]	RIRB Size		
				0001	16 B = 2 entries	1	
7:4	RO	Imp.Dep		0010	128 B = 16 entries		
				0100	2048 B = 256 Entries		
				1000	Reserved		
3:2					ter would be Read Only 0101b. rt more than one RIRB Size.		
0.2	RW	Imp.Dep	RIRB Size (RIRBSIZE): The setting of the register determines when the address counter in the DMA controller will wrap around.				
			address cour		· · · · · · · · · · · · · · · · · · ·	1	
				Bits [1:0]	RIRB Size		
				00	16 B = 2 entries		
				01	128 B = 16 entries		
:0				10	2 KB = 256 entries		
				11	Reserved		
			This value must not be changed when the RIRB DMA engine is enabled.				
			_	• • •	ed size will produce unspecified it is permissible to make this fiel		