

# Intel® High Definition Audio Specification Document Change Notification

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This document discloses changes to the Intel® High Definition Audio Specification and all information contained herein is provided under the terms of the "AZALIA" SPECIFICATION DEVELOPMENT AGREEMENT" also known as Intel® High Definition Audio Specification Developer Agreement, and all the terms of such agreement, including the confidentiality provisions, shall apply to this disclosure.

## Title: **HDMI High Bit Rate Support**

### Brief description of the functional changes:

This DCN provides a set of addition and changes to the HD Audio specification that defines how the HDMI high bit rate feature is declared and configured. Note that this DCN is built on top of the DCN No: HDA034-A for the feature addition.

### Definition Text Formatting:

xxx Original text in existing specification or DCN released earlier.  
yyy New text inserted by this new DCN.  
zzz Deleted text introduced by this new DCN.

### New Definitions:

#### 7.3.3.13 Pin Widget Control

Pin Widget Control controls several aspects of the Pin Widget.

#### Command Options:

Table 1. Enable VRef

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F07h	0	Bits 31:8 are 0 Bits 7:0 are PinCntl
Set	707h	Bits 7:0 are PinCntl	0

**PinCntl format:**

<b>7</b>	<b>6</b>	<b>5</b>	<b>4:3</b>	<b>2</b>	<b>1:0</b>
H-Phn Enable	Out Enable	In Enable	Rsvd	VRefEn[2]	VRefEn[1:0] / EPT

**Figure 63. PinCntl Format**

**H-Phn Enable** disables/enables a low impedance amplifier associated with the output. The value 1 enables the amp. Enabling a non-existent amp is ignored. For digital pin widgets, including HDMI, this control has no function.

**Out Enable** allows the output path of the Pin Widget to be shut off. The value 1 enables the path. Enabling a non-existent amp is ignored. For a digital HDMI pin widget, disabling the output will cause the samples to no longer be sent to the HDMI Sink device. Other signaling may continue, such as clock recovery and other Info Frame packets.

**In Enable** allows the input path of the Pin Widget to be shut off. The value 1 enables the path.

**VRefEn:** Voltage Reference Enable controls the VRef signal(s) associated with the **non digital** Pin Widget. If more than one of the bits in the VRef[7:0] field of the Pin Capabilities parameter (Section 7.3.4.9) are non-zero, then this control allows the signal level to be selected. **For digital pin widgets, including HDMI, this control has no function.**

The VRefEn field encoding selects one of the possible states for the VRef signal(s). If the value written to this control does not correspond to a supported value as defined in the Pin Capabilities parameter, the control must either retain the previous value or take the value of 000, which will put the control in a Hi-Z state and prevent damage to any attached components.

Table 82 enumerates the possible values for VRefEn which correlate to the values identified in the Pin Capabilities parameter (see Figure 89).

**Table 82. VRefEn Values**

VRefEn Encoding	VREF Signal Level
000b	Hi-Z
001b	50%
010b	Ground (0 V)
011b	<i>Reserved</i>
100b	80%
101b	100%
110b-111b	<i>Reserved</i>

**EPT:** Encoded Packet Type controls the packet type used to transmit the audio stream on the associated digital Pin Widget. Native audio packet type is always supported. If there are non native packet types supported as declared in the Pin Capabilities parameter (Section 7.3.4.9), then this control allows the encoded packet type to be selected.

The EPT field encoding selects one of the possible packet types for sending out on the digital Pin Widget. If the value written to this control does not correspond to a supported value as defined in the Pin

Capabilities parameter, the control must either retain the previous value or take the value of 00, which will select the default native audio packet type.

Table 83 enumerates the possible values for EPT which correlates to the supported type identified in the Pin Capabilities parameter (see Figure 77).

**Table 83. EPT Values**

EPT Encoding	Description
00b	Native. For HDMI Pin Widget, it indicates Audio Sample Packet.
01b-10b	<i>Reserved</i>
11b	High Bit Rate. For HDMI Pin Widget, it indicates HBR Audio Stream Packet.

**Applies to:**

- Pin Complex, both Digital (HDMI) and analog

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**7.3.3.35 Converter Channel Count**

The *Converter Channel Count* control is used by software to program the number of channels in the incoming stream that the converter must render.

**Command Options:**

	Verb ID	Payload (8 Bits)	Response (32 Bits)
<b>Get</b>	F2Dh	0	Converter Channel Count 7:0
<b>Set</b>	72Dh	Converter Channel Count 7:0	

**Figure 73. Converter Channel Count**

The Converter Channel Count control is used to specify the number of active channels in the audio stream. It is used in conjunction with the Channel value set in the Converter Stream, Channel control to specify which channels in an incoming audio stream are to be decoded by the codec. Converter Channel Count is 0-indexed as is Channel value in the Converter Stream, Channel control.

For the example below, allow S to be the Channel value in the Converter Stream, Channel control, and C to be the Converter Channel Count. Assume two channels intended for stereo playback are destined for a codec in a stream with greater than two total channels.

Assuming the first channel to be decoded is stream position 3:

$$S = 2$$

For Stereo, 2 streams are required:

$$C = 1$$

The codec would then output a stereo stream using the third and fourth channels in the incoming stream.

Note that when using the digital output converter pairing with HDMI Pin Widget configured for sending HBR packet type, the converter channel count must be programmed to 8. Per HDMI specification, these HBR audio streams will be packetized into 128 bit chunks when transmitted over HDMI. On the other hand HD Audio specification today only support up to 192 KHz frame rate, hence, these HBR audio streams will have to be transmitted as 8 channels of 16 bit data with 192 KHz frame rate (24.576 Mbps), or 8 channels of 16 bit data with 96 KHz frame rate (12.288 Mbps), over HD Audio Link. The mapping of the 8 channels of HBR audio stream over HD Audio Link to the 128 bit chunks HBR audio stream over HDMI will be carried out according to the sequence order of samples arriving.

**Applies to:**

- HDMI Output Converter

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**7.3.4.9 Pin Capabilities**

The Pin Capabilities parameter returns a bit field describing the capabilities of the Pin Complex Widget.

**Parameter ID:** 0Ch

**Response Format:**

<b>31:28</b>	<b>27</b>	<b>31:26:17</b>	<b>16</b>	<b>15:8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<i>Rsvd</i>	<b>HBR</b>	<i>Rsvd</i>	EAPD Capable	VRef Control	HDMI	Balanced I/O Pins	Input Capable	Output Capable	Headphone Drive Capable	Presence Detect Capable	Trigger Req'd	Impedance Sense Capable

**Figure 89. Pin Capabilities Response Format**

**HBR (High Bit Rate)** indicates the pin widget capability in sending out audio stream using High Bit Rate packet. Capable if set to 1. This bit is only applicable for HDMI pin widget.

**EAPD Capable** indicates the codec has an EAPD pin and that this Pin Widget provides support for controlling that pin.

**VRef Control[7:0]** is a bit field used to indicate what voltages may be produced on the associated VRef pin(s). If all bits in the bit field are 0, then VRef generation is not supported by the Pin Complex. Also, if the Input Capable bit is a 0, then the VRef bit field has no meaning and all bits must be 0.

If the Output Capable bit and any bits in the VRef field are set, then bit 0 (Hi-Z) must also be set to indicate that the VRef signal can be turned off to support output devices.

Figure 90 describes the VRef bit field. A 1 in any position indicates that the associated signal level is supported. All values of VRef are specified as a percentage of the analog voltage rail, AVdd.

<b>7:6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<i>Rsvd</i>	100%	80%	<i>Rsvd</i>	Ground	50%	Hi-Z

**Figure 90. VRef Bit Field**

**HDMI** indicates that the Pin Complex Widget supports connection to a HDMI Sink.

**Balanced I/O Pins** indicates that the Pin Complex Widget has balanced pins.

**Input Capable** indicates whether the pin complex supports input. If Input Capable is a 1, the pin is capable of input.

**Output Capable** indicates whether the pin complex supports output. If Output Capable is a 1, the pin is capable of output.

**Headphone Drive Capable** indicates that the pin has an amplifier with sufficient current drive to drive headphones. If Output Capable is a 0, then this bit has no meaning and must be 0.

**Presence Detect Capable** indicates whether the pin complex can perform presence detect to determine whether there is anything plugged in. Presence detect does not indicate *what* is plugged in, only that *something* is plugged in.

**Trigger Required** indicates whether a trigger is required for an impedance measurement (see Section **Error! Reference source not found.**).

**Impedance Sense Capable** indicates whether the pin complex supports impedance sense on the attached peripheral to determine what it is. More accurate (possibly sequenced) forms of peripheral discrimination may be supported independent of this capability; however, if this bit is a 1, then the codec must support at least the basic impedance test as described in Section **Error! Reference source not found.**

**Applies to:**

- Pin Widget