Intel® High Definition Audio Specification
Document Change Notification

Date:	December 8, 2005		
Company:	Intel Corporation		
Address:	1900 Prairie City Rd.		
City:	Folsom	State:	CA
Country:	USA	Zip:	95630

Change Identification:	**DCN No: HDA001-A**
Document Revision:	Intel® High Definition Audio 1.0

Title: Clarification to Interrupt Status

Brief description of the functional changes:

The Intel® High Definition Audio specification version 1.0 specifies that Interrupt Status bits CIS and SIS are sticky and written to 1 to clear, but with the known implementations CIS and SIS are an OR of the interrupt condition and can not be cleared by writing a 1. As current implementations differ from the specification the specification is updated to reflect the real world implementations.

Current Definition:

Section 3.3.14 and 3.3.15 of the Intel® High Definition specification version 1.0 defines:

3.3.14 Offset 20h: INTCTL – Interrupt Control

Length: 4 bytes

Table 1. Interrupt Control Register

Bit	Type	Reset	Description
31	RW	0	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. When set to 1, the High Definition Audio device is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space.
30	RW	0	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. When set to 1 the controller generates an interrupt when the corresponding status bit get sets due to a Response Interrupt, a Response Buffer Overrun, and wake events.
29:0	RW	0h	**Stream Interrupt Enable (SIE):** When set to 1, the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC = 1 in the BDL entry being completed or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. For instance, if there are two input streams, three output streams, and one bidirectional stream (ISS = 2, OSS = 3, BSS = 1), the bit assignments would be as follows: Bit 0: Input Stream 1 Bit 1: Input Stream 2 Bit 2: Output Stream 1 Bit 3: Output Stream 2 Bit 4: Output Stream 3 Bit 5: Bidirectional Stream 1 Bits 6-28: *Reserved*

3.3.15 Offset 24h: INTSTS – Interrupt Status

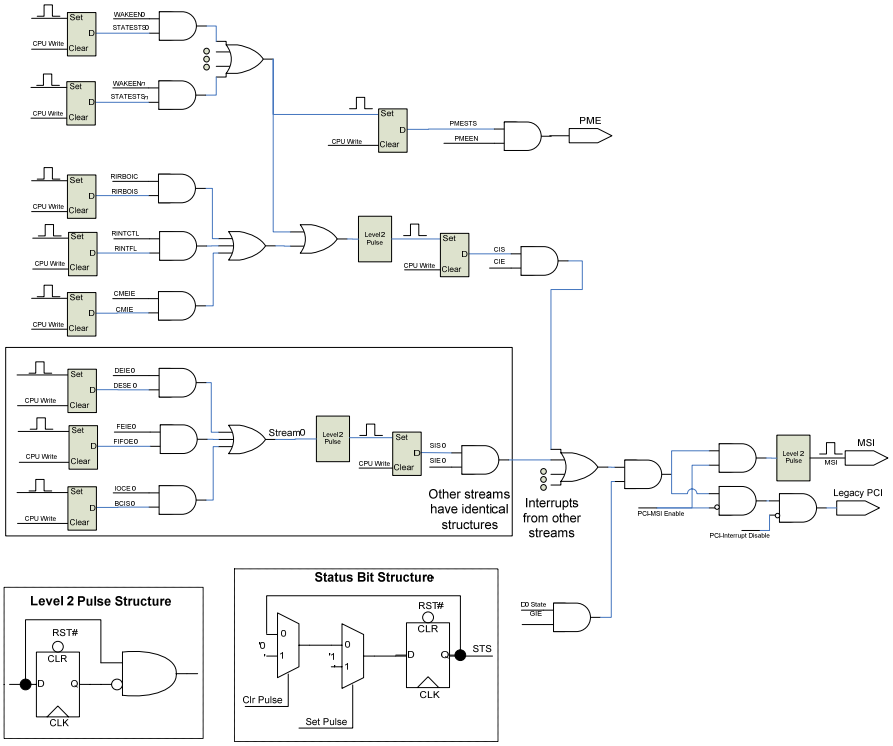
Length: 4 bytes

Table 2. Interrupt Status Register

Bit	Type	Reset	Description
31	RO	0	**Global Interrupt Status (GIS):** This bit is an “OR” of all of the interrupt status bits in this register.

30	RW1C	0	**Controller Interrupt Status (CIS):** Status of general controller interrupt. This bit may be set regardless of the corresponding enable bit, but a hardware interrupt will not be generated unless the corresponding enable bit is set. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Overrun, or a Codec State Change request. The exact cause can be determined by interrogating the RIRB Status register and the State Change Status register. Note that this bit is set regardless of the state of the corresponding interrupt enable bit. This bit is cleared by writing a 1.
29:0	RW1C	0h	**Stream Interrupt Status (SIS):** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that these status bits are set regardless of the state of the corresponding interrupt enable bits. The bits are cleared by writing 1's to them. The streams are numbered and the SIS bits assigned sequentially based on their order in the register set in the same way the SIE bits are set. (Section 0).

Section 3.5 of the Intel® High Definition specification version 1.0 defines:



New Definition:

3.3.14 Offset 20h: INTCTL – Interrupt Control

Length: 4 bytes

Table 3. Interrupt Control Register

Bit	Type	Reset	Description
31	RW	0	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. When set to 1, the High Definition Audio device is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space.
30	RW	0	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. When set to 1 the controller generates an interrupt when the corresponding status bit get sets due to a Response Interrupt, a Response Buffer Overrun, and wake events.
29:0	RW	0h	**Stream Interrupt Enable (SIE):** When set to 1, the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC = 1 in the BDL entry being completed or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. For instance, if there are two input streams, three output streams, and one bidirectional stream (ISS = 2, OSS = 3, BSS = 1), the bit assignments would be as follows: Bit 0: Input Stream 1 Bit 1: Input Stream 2 Bit 2: Output Stream 1 Bit 3: Output Stream 2 Bit 4: Output Stream 3 Bit 5: Bidirectional Stream 1 Bits 6-28: *Reserved* All bits not assigned to a supported DMA engine are RsvdZ.

3.3.15 Offset 24h: INTSTS – Interrupt Status

Length: 4 bytes

Table 4. Interrupt Status Register

Bit	Type	Reset	Description
31	RO	0	**Global Interrupt Status (GIS):** This bit is an “OR” of all of the interrupt status bits in this register.

30	RO	0	**Controller Interrupt Status (CIS):** Status of general controller interrupt. This bit may be set regardless of the corresponding enable bit, but a hardware interrupt will not be generated unless the corresponding enable bit is set. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Overrun, or a Codec State Change request. The exact cause can be determined by interrogating the RIRB Status register and the State Change Status register. Note that this bit is set regardless of the state of the corresponding interrupt enable bit. ~~This bit is cleared by writing a 1.~~
29:0	RO	0h	**Stream Interrupt Status (SIS):** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that these status bits are set regardless of the state of the corresponding interrupt enable bits. ~~The bits are cleared by writing 1's to them.~~ The streams are numbered and the SIS bits assigned sequentially based on their order in the register set in the same way the SIE bits are set. (Section 0).

Section 3.5

Error! Reference source not found. is a representation of the interrupt tree to show the logical relationship of various signals. It should not be taken as a literal implementation.