Intel® High Definition Audio Specification
Document Change Notification

Date: November 15, 2006

Change Identification: **DCN No: HDA024-A**
Document Revision: Intel® High Definition Audio 1.0

Title: Addition of Dual Voltage Interface Support

Brief description of the functional changes proposed:

This ECR replaces completely Chapter 6 of the Intel® High Definition Audio 1.0 Specification and adds the capability to the HD Audio interface to support either 3.3V or 1.5V signaling. The proposed definition would allow the board designer to decide the signaling level of the High Definition Audio interface. All components on the High Definition Audio link should support 3.3V signaling, 1.5V signaling is an optional feature.

Current Definition:

HD Audio interface supports 3.3V signaling only.

Proposed Definition:

Adds capability to the HD Audio interface to support either 3.3V or 1.5V signaling.

6.0 Electrical Interface

6.1 Overview

This chapter defines the electrical characteristics and constraints of High Definition Audio link. It is divided into sections covering integrated circuit component & system specification and physical requirements. Each section contains the requirements that must be met by the respective product, as well as the assumptions it may make about the environment provided. While every attempt was made to make these sections self-contained, there are invariably dependencies between sections so that it is necessary that all vendors be familiar with all areas.

The 1.5V and 3.3v signaling details of the High Definition Audio interface have been included in this revision.

6.1.1 3.3V to Low Voltage (1.5V) Transition

One goal of High Definition Audio is to provide a quick and easy transition from 3.3V signaling to low voltage signaling (1.5V) on the electrical link.

The motherboard defines the signaling environment for the High Definition Audio link, whether it is 3.3V or 1.5V. The 3.3V board is designed to work only with High Definition Audio components that are capable of 3.3V signaling. Similarly the low voltage board is designed to work only with High Definition Audio components that are designed to support low voltage signaling. However, it is recommended that components on the High Definition Audio link are designed such that they are capable of working in either of these two signaling environments.

6.2 3.3V Signaling Environment

This section defines the electrical characteristics of High Definition Audio components for 3.3V signaling scheme. The 3.3V High Definition Audio components can be designed with standard CMOS I/O technology. Unless specifically stated otherwise, component parameters apply at the package pins; not at bare silicon pads nor at card edge connectors.

6.2.1 DC Specifications

The DC specifications of the 3.3V High Definition Audio components are summarized in Table 1.

Table 1: 3.3V DC specification

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vcc	Supply Voltage		3.135	3.465	V	
Vih	Input High Voltage		0.65xVcc		V	
Vil	Input Low Voltage			0.35xVcc	V	
Voh	Output High Voltage	Iout =-500uA	0.9xVcc		V	
Vol	Output Low Voltage	Iout =1500uA		0.10xVcc	V	
Iil	Input Leakage Current	0<Vin<Vcc		±10	uA	1
Cin	Input Pin Capacitance			7.5	pF	
Lpin	Pin Inductance			20	nH	2

NOTES:

1. For **SDI** buffers (or in general any bi-directional buffer with tri-state output), input leakage current also include hi-Z output leakage.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

6.2.2 AC Specifications

The output driver on the High Definition Audio electrical link must be able to deliver an initial voltage of at least Vil or Vih respectively at the receiver through the bus with known characteristic impedance and at the same time meeting signal quality requirements.

The minimum and maximum drive characteristics of High Definition Audio output buffers are defined by the V/I curves. Figure 1 and Table 2 describe the **SDO** buffer AC drive specification where as the Figure 2 and Table 3 describe the AC drive specification of the SDI buffers. The AC drive specification for **SYNC**, **RST#** and **BCLK** buffers is same as that of **SDO**.

These curves should be interpreted as traditional 'DC' transistor curves with the following exceptions: 'DC drive point' is the only position on the curves at which steady state operation is intended, while the higher currents are only reached momentarily during bus switching transients. The 'AC drive point' (real definition of buffer strength) defines the minimum instantaneous current required to switch the bus.

Adherence to these curves should be evaluated at worst case conditions. Minimum pull up curve is evaluated at minimum Vcc and high temperature. Minimum pull down curve is evaluated at minimum Vcc and high temperature. The maximum curve test points are evaluated at maximum Vcc and low temperature.

Inputs must be clamped to both ground and power rails. The clamp diode characteristics are also listed here for reference.

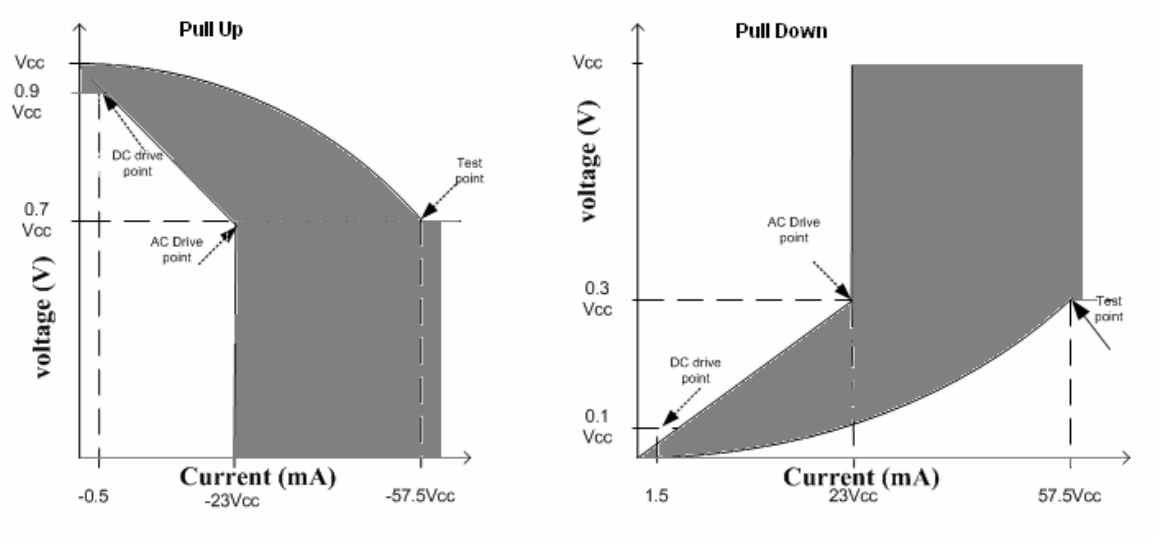

Figure 1: V/I Curves for SDO buffers

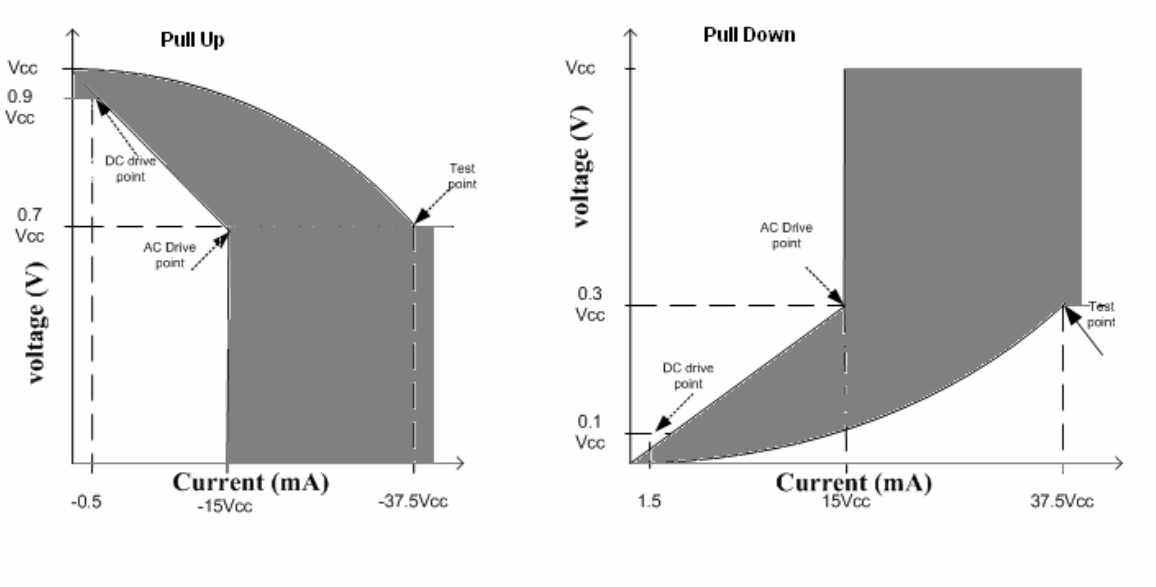

Figure 2: V/I Curves for SDI buffers

Equation C

Ioh = (174.2/Vcc)*(Vout-Vcc)*(Vout+0.4Vcc) ; for Vcc > Vout > 0.7 Vcc

Equation D

Iol = (273.8/Vcc)*Vout*(Vcc-Vout) ; for 0v < Vout < 0.3 Vcc

Equation E

Ioh = (113.6/Vcc)*(Vout-Vcc)*(Vout+0.4Vcc) ; for Vcc > Vout > 0.7 Vcc

Equation F

Iol = (178.6/Vcc)*Vout*(Vcc-Vout) ; for 0v < Vout < 0.3 Vcc

Table 2: SDO buffer AC specification

Symbol	Parameter	Condition	Min	Max	Units
Ioh (AC)	Switching Current high	0 < Vout < 0.7vcc	-23Vcc		mA
		0.7Vcc < Vout < 0.9Vcc	-76.7(Vcc-Vout)		
		0.7Vcc < Vout < Vcc		Eqt'n C	
	(Test Point)	Vout = 0.7Vcc		-57.5Vcc	
Iol (AC)	Switching Current Low	Vcc > Vout >0.3Vcc	23Vcc		mA
		0.3Vcc > Vout > 0.1Vcc	76.7Vout		mA
		0.3Vcc > Vout > 0		Eqt'n D	mA
	(Test Point)	Vout = 0.3Vcc		57.5Vcc	mA
Icl	Low Clamp Current	-3 < Vin < -1	-25+(Vin+1)/0.015		mA
Ich	High Clamp Current	Vcc+4 > Vin > Vcc+1	25+(Vin-Vcc-1)/0.015		mA

slew_r	Output rise Slew rate	0.25Vcc to 0.75Vcc	1	3	V/ns (note1)
slew_f	Output rise Slew rate	0.75Vcc to 0.25Vcc	1	3	V/ns (note1)

Table 3: SDI buffer AC specification

Symbol	Parameter	Condition	Min	Max	Units
Ioh (AC)	Switching Current high	0 < Vout < 0.7vcc	-15Vcc		mA
		0.7Vcc < Vout < 0.9Vcc	-50(Vcc-Vout)		
		0.7Vcc < Vout < Vcc		Eqt'n E	
	(Test Point)	Vout = 0.7Vcc		-37.5Vcc	
Iol (AC)	Switching Current Low	Vcc > Vout >0.3Vcc	15Vcc		mA
		0.3Vcc > Vout > 0.1Vcc	50Vout		mA
		0.3Vcc > Vout > 0		Eqt'n F	mA
	(Test Point)	Vout = 0.3Vcc		37.5Vcc	mA
Icl	Low Clamp Current	-3 < Vin < -1	-25+(Vin+1)/0.015		mA
Ich	High Clamp Current	Vcc+4 > Vin > Vcc+1	25+(Vin-Vcc-1)/0.015		mA
slew_r	Output rise Slew rate	0.25Vcc to 0.75Vcc	1	3	V/ns (note 1)
slew_f	Output rise Slew rate	0.75Vcc to 0.25Vcc	1	3	V/ns (note 1)

NOTES:

1. Slew rate is to be interpreted as the cumulative edge rate across the specified range, (0.25Vcc to 0.75Vcc load for rise and 0.75Vcc to 0.25Vcc load for fall), rather than instantaneous rate at any point within the transition range. Section 6.4 Measurements and test conditions, specifies the load used to characterize the slew rates. This requirement for the slew rate applies to all the output buffers on the High Definition Audio link.

6.2.3 Maximum AC Ratings and Device Protection

All High Definition Audio buffers should be capable of withstanding continuous exposure to the waveform shown in Figure 3. It is recommended that these waveforms be used as qualification criteria against which the long term reliability of each device is evaluated. Table 4 lists the parameters of the waveform. This level of robustness should be guaranteed by design; it is not intended that this waveform should be used as a production test.

These waveforms are applied with the equivalent of a zero impedance voltage source, driving through a series resistor directly into each High Definition Audio input or tri-stated output pin. The open-circuit voltage of the voltage source is shown in Figure 3, which is based on the worst case overshoot and undershoot expected in actual High Definition Audio buses. The resistor values are calculated to produce the worst case current into an effective internal clamp diode.

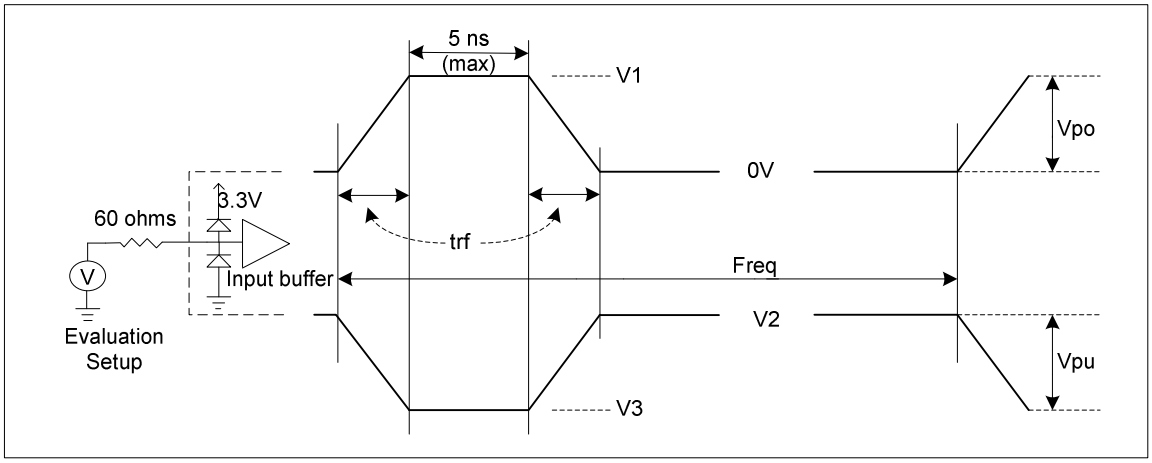

Figure 3: Maximum AC waveforms for 3.3V signaling

Table 4: Parameters for Maximum AC signaling waveforms

Symbol	Parameter	Min	Max	Units
V1	Overshoot Voltage		6.3	V
V2	Undershoot initial Voltage		3.465	V
V3	Undershoot Voltage	-3		V
Vpu	Waveform peak-to-peak		6.465	V
Vpo	Waveform peak-to-peak		6.3	V
trf	Rise/fall time	1	3	V/ns
Freq	Frequency of AC rating waveform as applied to SDI input buffers		24	MHz
Freq	Frequency of AC rating waveform as applied to SDO input buffers		24	MHz

Note that:

- The voltage waveform is supplied at the resistor shown in the evaluation setup, not the package pin.
- Any internal clamping in the device being tested will greatly reduce the voltage levels seen at the package pin.

6.3 Low Voltage Signaling Environment

This section defines the electrical characteristics of High Definition Audio components for 1.5V signaling. Unless specifically stated otherwise, component parameters apply at the package pins; not at bare silicon pads nor at card edge connectors.

6.3.1 DC Specifications

The DC specifications of the 1.5V High Definition Audio components are summarized in Table 5

Table 5: 1.5V DC specification

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vcc	Supply Voltage		1.418	1.583	V	
Vih	Input High Voltage		0.6xVcc		V	
Vil	Input Low Voltage			0.4xVcc	V	
Voh	Output High Voltage	Iout =-500uA	0.9xVcc		V	
Vol	Output Low Voltage	Iout =1500uA		0.10xVcc	V	
Iil	Input Leakage Current	0<Vin<Vcc		±10	uA	1
Cin	Input Pin Capacitance			7.5	pF	
Lpin	Pin Inductance			20	nH	2

NOTES:

1. For **SDI** buffers (or in general any bi-directional buffer with tri-state output), input leakage current also include hi-Z output leakage.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

6.3.2 AC Specifications

The output driver on the High Definition Audio electrical link must be able to deliver an initial voltage of at least Vil or Vih respectively at the receiver through the bus with known characteristic impedance and at the same time meeting signal quality requirements.

The minimum and maximum drive characteristics of High Definition Audio output buffers are defined by the V/I curves. Table 6 and Figure 4 describe the **SDO** buffer AC drive specification where as the Table 7 and Figure 5 describe the AC drive specification of the SDI buffers. The AC drive specification for **SYNC**, **RST#** and **BCLK** buffers is same as that of **SDO**.

These curves should be interpreted as traditional ‘DC’ transistor curves with the following exceptions: ‘DC drive point’ is the only position on the curves at which steady state operation is intended, while the higher currents are only reached momentarily during bus switching transients. The ‘AC drive point’ (real definition of buffer strength) defines the minimum instantaneous current required to switch the bus.

Adherence to these curves should be evaluated at worst case conditions. Minimum pull up curve is evaluated at minimum Vcc and high temperature. Minimum pull down curve is evaluated at minimum Vcc and high temperature. The maximum curve test points are evaluated at maximum Vcc and low temperature.

Inputs must be clamped to both ground and power rails. The clamp diode characteristics are also listed here for reference.

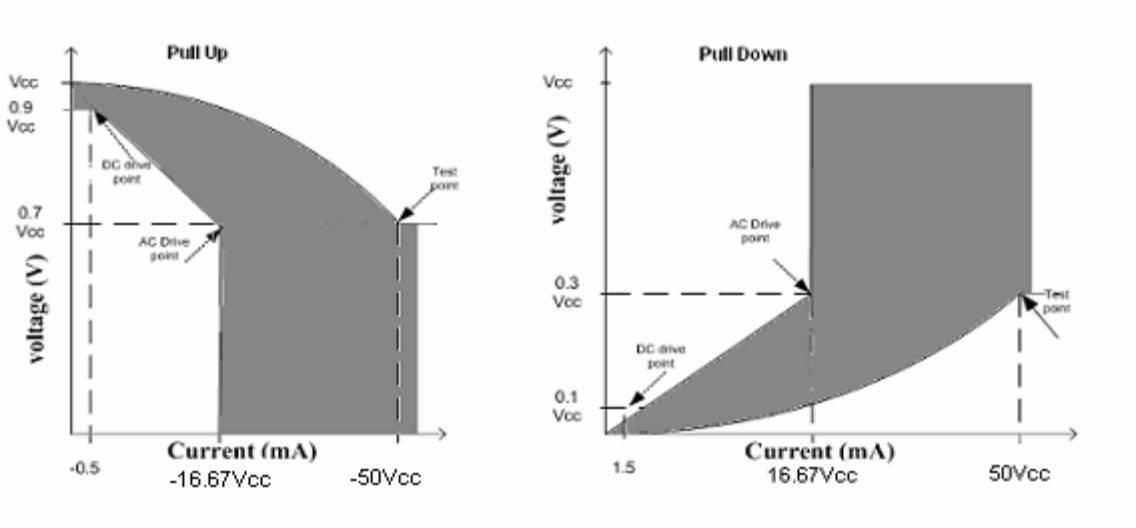

Figure 4: V/I Curves for SDO buffers

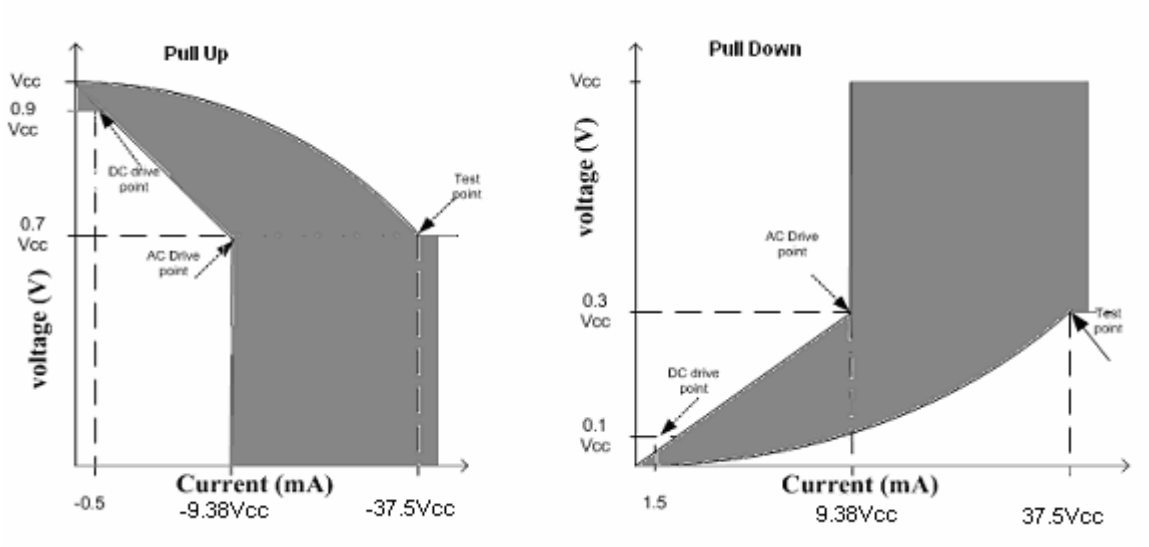

Figure 5: V/I Curves for SDI buffers

Equation C

Ioh = (151.52/Vcc)*(Vout-Vcc)*(Vout+0.4Vcc) ; for Vcc > Vout > 0.7 Vcc

Equation D

Iol = (238.1/Vcc)*Vout*(Vcc-Vout) ; for 0v < Vout < 0.3 Vcc

Equation E

Ioh = (113.64/Vcc)*(Vout-Vcc)*(Vout+0.4Vcc) ; for Vcc > Vout > 0.7 Vcc

Equation F

Iol = (178.57/Vcc)*Vout*(Vcc-Vout) ; for 0v < Vout < 0.3 Vcc

Table 6: SDO buffer AC specification

Symbol	Parameter	Condition	Min	Max	Units
Ioh (AC)	Switching Current high	0 < Vout < 0.7vcc	-16.67Vcc		mA
		0.7Vcc < Vout < 0.9Vcc	-55.57(Vcc-Vout)		
		0.7Vcc < Vout < Vcc		Eqt'n C	
	(Test Point)	Vout = 0.7Vcc		-50Vcc	
Iol (AC)	Switching Current Low	Vcc > Vout >0.3Vcc	16.67Vcc		mA
		0.3Vcc > Vout > 0.1Vcc	55.57Vout		mA
		0.3Vcc > Vout > 0		Eqt'n D	mA
	(Test Point)	Vout = 0.3Vcc		50Vcc	mA
Icl	Low Clamp Current	-3 < Vin < -1	-25+(Vin+1)/0.015		mA
Ich	High Clamp Current	Vcc+4 > Vin > Vcc+1	25+(Vin-Vcc-1)/0.015		mA
slew_r	Output rise Slew rate	0.25Vcc to 0.75Vcc	0.5	1.5	V/ns (note1)
slew_f	Output rise Slew rate	0.75Vcc to 0.25Vcc	0.5	1.5	V/ns (note1)

Table 7: SDI buffer AC specification

Symbol	Parameter	Condition	Min	Max	Units
Ioh (AC)	Switching Current high	0 < Vout < 0.7vcc	-9.38Vcc		mA
		0.7Vcc < Vout < 0.9Vcc	-31.27(Vcc-Vout)		
		0.7Vcc < Vout < Vcc		Eqt'n E	
	(Test Point)	Vout = 0.7Vcc		-37.5Vcc	
Iol (AC)	Switching Current Low	Vcc > Vout >0.3Vcc	9.38Vcc		mA
		0.3Vcc > Vout > 0.1Vcc	31.27Vout		mA
		0.3Vcc > Vout > 0		Eqt'n F	mA
	(Test Point)	Vout = 0.3Vcc		37.5Vcc	mA
Icl	Low Clamp Current	-3 < Vin < -1	-25+(Vin+1)/0.015		mA
Ich	High Clamp Current	Vcc+4 > Vin > Vcc+1	25+(Vin-Vcc-1)/0.015		mA
slew_r	Output rise Slew rate	0.25Vcc to 0.75Vcc	0.5	1.5	V/ns (note 1)
slew_f	Output rise Slew rate	0.75Vcc to 0.25Vcc	0.5	1.5	V/ns (note 1)

NOTES:

1. Slew rate is to be interpreted as the cumulative edge rate across the specified range, (0.25Vcc to 0.75Vcc load for rise and 0.75Vcc to 0.25Vcc load for fall), rather than instantaneous rate at any point within the transition range. Section 6.4 Measurements and test conditions, specifies the load used to characterize the slew rates. This requirement for the slew rate applies to all the output buffers on the High Definition Audio link.

6.3.3 Maximum AC Ratings and Device Protection

All High Definition Audio buffers should be capable of withstanding continuous exposure to the waveform shown in Figure 6. It is recommended that these waveforms be used as qualification criteria against which the long term reliability of each device is evaluated. Table 8 and Table 9 list the parameters of the waveform. This level of robustness should be guaranteed by design; it is not intended that this waveform should be used as a production test.

These waveforms are applied with the equivalent of a zero impedance voltage source, driving through a series resistor directly into each High Definition Audio input or tri-stated output pin. The open-circuit voltage of the voltage source is shown in Figure 6, which is based on the worst case overshoot and undershoot expected in actual High Definition Audio buses for 1.5V signaling. The resistor values are calculated to produce the worst case current into an effective internal clamp diode.

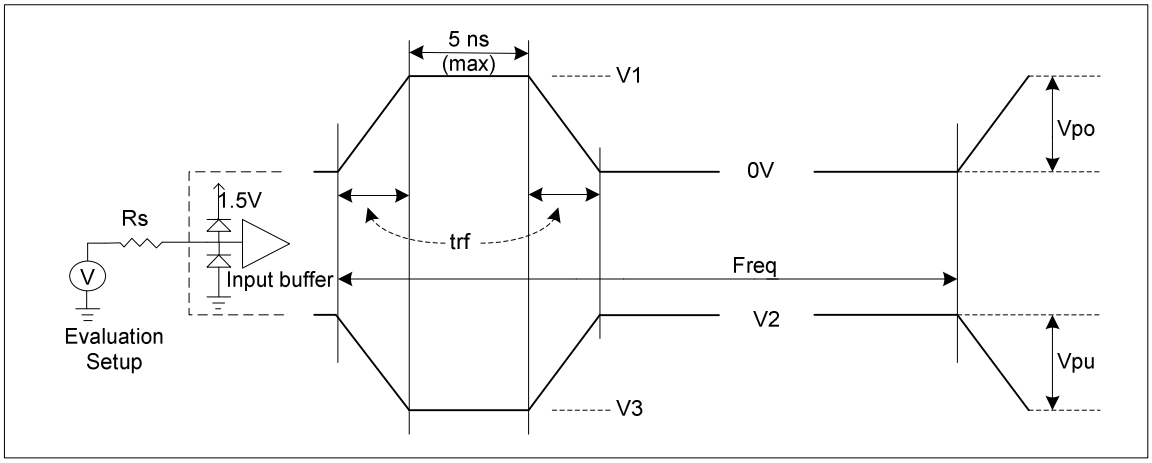

Figure 6: Maximum AC waveforms for 1.5V signaling

Table 8: Parameters for Maximum AC signaling waveforms

Symbol	Parameter	Min	Max	Units
V1	Overshoot Voltage		3.25	V
V2	Undershoot initial Voltage		1.65	V
V3	Undershoot Voltage	-1.6		V
Vpu	Waveform peak-to-peak		3.25	V
Vpo	Waveform peak-to-peak		3.25	V
trf	Rise/fall time	0.5	1.5	V/ns
Freq	Frequency of AC rating waveform as applied to SDI input buffers		24	MHz
Freq	Frequency of AC rating waveform as applied to SDO input buffers		24	MHz

Table 9: Resistance value for the AC rating waveform

Rs	Condition	Value
	Overshoot waveform at the Codec	65 ohms
	Undershoot waveform at the Codec	101 ohms
	Overshoot waveform at the Controller	108 ohms
	Undershoot waveform at the Controller	133 ohms

Note that:

- The voltage waveform is supplied at the resistor shown in the evaluation setup, not the package pin.
- Any internal clamping in the device being tested will greatly reduce the voltage levels seen at the package pin.

6.4 Measurements and test conditions

Figure 9 and Figure 10 define the timing parameters as measured at the controller and the codec respectively. The component test guarantees that all timings are met with minimum clock slew rate (slowest edge) and minimum voltage swing. The design must guarantee that minimum timings are also met with maximum clock slew rate (fastest edge) and maximum voltage swing. In addition, the design must guarantee proper input operation for input voltage swings and slew rates that exceed the specified test conditions. The measurement conditions are summarized in Table 10. Figure 7and Figure 8 specify the load used to characterize the slew rates and delay time. The reference point for all delay timing measurements is 0.5Vcc.

The load used to characterize the slew rate and the delay is the same for both 1.5V and 3.3V signaling.

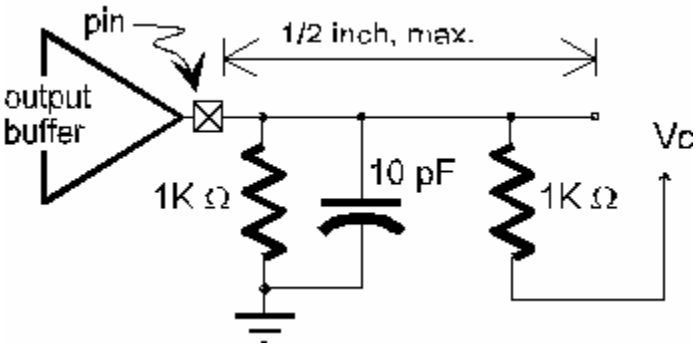

Figure 7: Slew rate and min valid delay

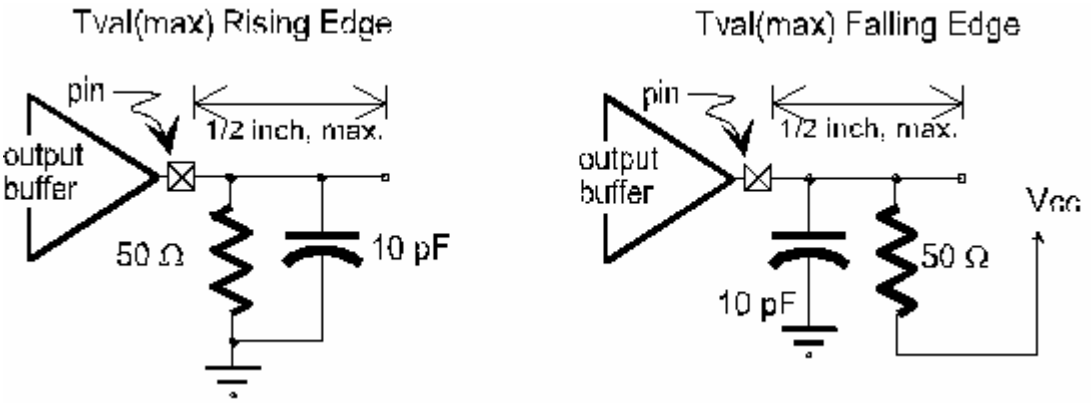

Figure 8: Max valid delay

Table 10: Measurement condition parameters

Symbol	1.5V signaling	3.3V signaling	Units
V_h	0.7Vcc	0.75Vcc	V (note 1)
V_l	0.3Vcc	0.25Vcc	V (note1)
V_test	0.5Vcc	0.5Vcc	V
V_max	0.5Vcc	0.5Vcc	V (note 2)

NOTES:

1. Input test is done with 0.1Vcc of overdrive.

   V_h = Vih + 0.1 Vcc; V_l = Vil - 0.1 Vcc

2. V_max specifies the maximum peak to peak waveform allowed for measuring input timing

6.5 Timing Specification

6.5.1 Timing Parameters

Table 11describes the timing parameters at the controller interface and Table 12 describes the timing parameters at the codec interface. All the timing numbers are defined at the package pins of the corresponding interface. Rise and fall time, flight and delay time, setup and hold time listed here should be used together in the worst case scenario for modeling of the drivers on the High Definition Audio link. Setup and hold timing numbers for **SDO** are defined at every edge of the **BCLK** while those for **SDI** will be defined only at the rising edge of **BCLK**. This is due to the fact that **SDO** is double pumped while **SDI** is not. SYNC and RST# should be treated same as **SDO** and hence have the same timing definitions as that of **SDO**. Section 0 describes the method and the loads used to characterize these timing parameters.

Timing parameters and their values as defined here applies for both 3.3V as well as 1.5V signaling.

Table 11: Timing parameters at the controller

Symbol	Definition	Min	Typ	Max	Units	Notes
	BCLK frequency	23.9976	24.0	24.0024	MHz	3
T_cyc	Total period of BCLK	41.363	41.67	41.971	ns	3
T_high	High phase of BCLK	18.75		22.91	ns	1
T_low	Low phase of BCLK	18.75		22.91	ns	1
	BCLK jitter		150	300	ps	
T_ival	Time duration for which SDO is valid before the BCLK edge	7			ns	4
T_val	Time duration for which SDO is valid after the BCLK edge	7			ns	4
T_su	Setup for SDI at rising edge of the BCLK	15			ns	4
T_h	Hold for SDI at rising edge of the BCLK	0			ns	4

Table 12: Timing parameters at the codec

Symbol	Definition	Min	Typ	Max	Units	Notes
	BCLK frequency	23.9976	24.0	24.0024	MHz	3
T_cyc	Total period of BCLK	41.163	41.67	42.171	ns	3
T_high	High phase of BCLK	17.5		24.16	ns	2
T_low	Low phase of BCLK	17.5		24.16	ns	2
	BCLK jitter		150	500	ps	
T_tco	Time after rising edge of the BCLK that SDI becomes valid	3		11	ns	4
T_su	Setup for SDO at both rising and falling edge of the BCLK	5			ns	4
T_h	Hold for SDO at both rising and falling edge of the BCLK	5			ns	4

NOTES:

1. 45 / 55 % is the worst case duty cycle at the controller, as measured at v_test in Figure 9.
2. 42 / 58 % is the worst case duty cycle at the codec, as measured at v_test in Figure 10.
3. This is the long term average frequency measured over 1 ms. Clock has a 100 ppm tolerance in High Definition Audio interface.
4. The design should meet the timing requirements with the slew rate of the inputs in the range 1V/ns to 3 V/ns for 3.3V signaling and 0.5 V/ns to 1.5 V/ns for 1.5V signaling.

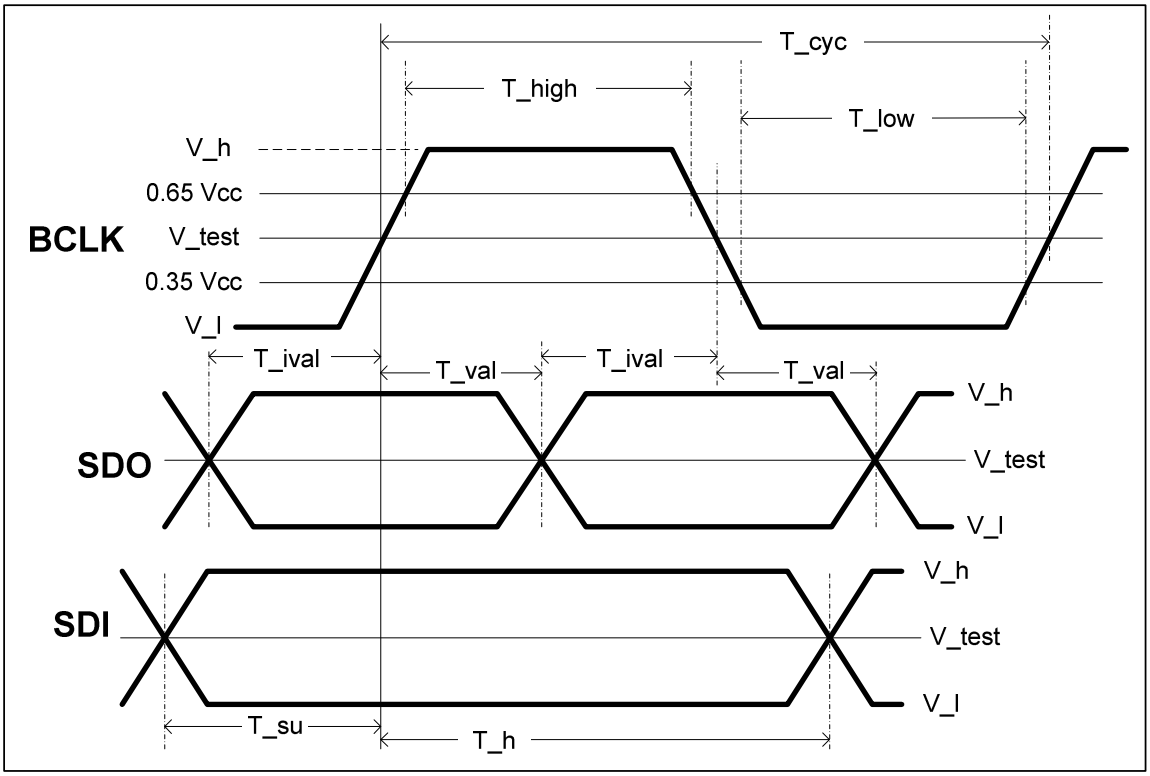

Figure 9: Timing parameters as measured at the controller

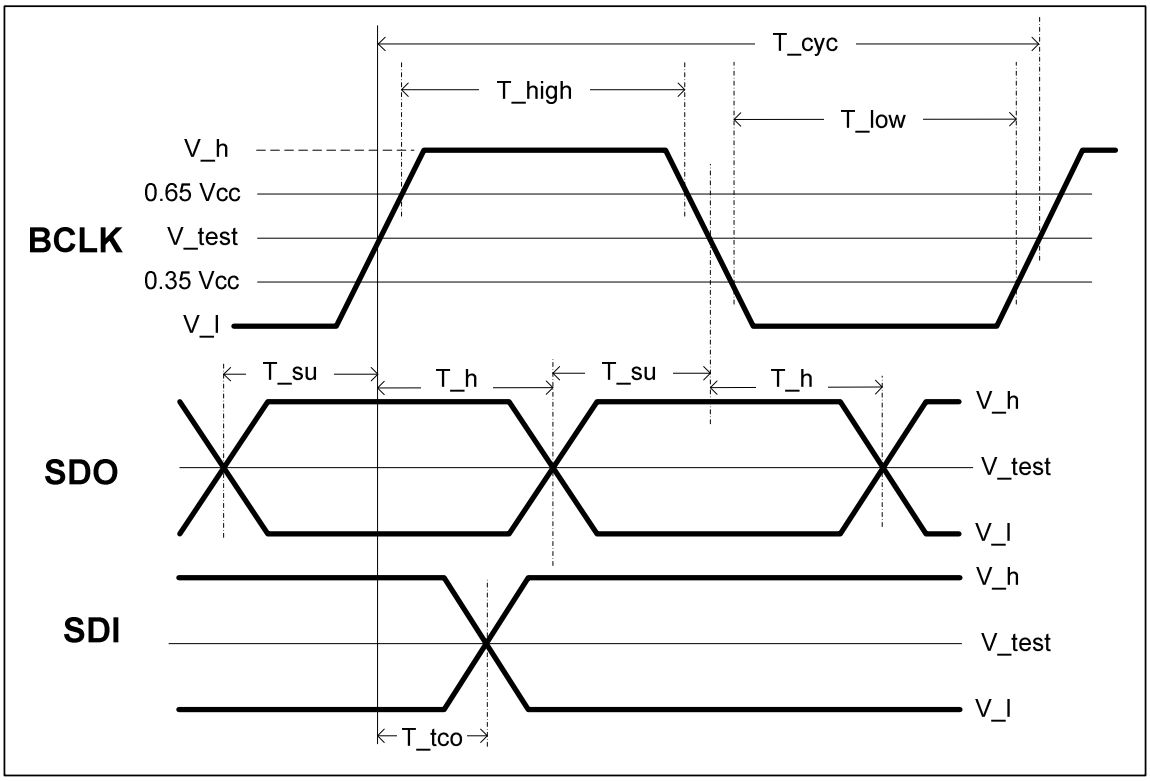

Figure 10: Timing parameters as measured at the codec

6.6 Vendor Provided Specification

The vendor of a High Definition Audio system is responsible for electrical simulation of the High Definition Audio link and components to guarantee proper operation. To help facilitate this effort, component vendors are encouraged to make the following information available: (It is recommended that component vendors make this information electronically available in the IBIS model format)

- All parasitic parameters for the package and the die as seen at the codec package pin
- Output static V/I curves and V/T under switching conditions. Two curves should be given for each output type used: one for driving high, the other for driving low. Both should show best-typical-worst curves.
- Input V/I characteristics. “Beyond-the-rail" response is critical, especially for inputs. The voltage range should span -3.3V to 6.6V for 3.3V signaling and correspondingly for 1.5V signaling.
- Rise/fall slew rates for each output type
- Complete absolute maximum data, including operating and non-operating temperature, DC maximums, etc.

6.7 System (Motherboard) Specification

System designers should be aware that with the increased driver strengths required to meet AC timings and signal integrity requirements, system routing may require system signal integrity improvement techniques, such as series resistors. It is the

system designer's responsibility to ensure compliance to this interface specification, taking into account the fact that this is a multi-drop scheme. This can be accomplished by simulating and validating the applicable topology configurations and making sure signal quality and timing requirements are met.

This section covers the topologies that were investigated to validate this specification. While these topologies offer a proof-of-concept for a range of configurations, they are not intended to replace proper system validation of specific system designs.

6.8 Power Requirements

It is recommended that the motherboard connects all High Definition Audio components with the same power supply voltages to the same power supply source and to a common ground plane to ensure minimum differences among their respective power supply and ground levels. Using a local supply voltage when the system supplied voltages are not available is permitted as long as the ground remains common. Proper decoupling methods must be used to ensure stable power supply and ground. Special consideration has to be made to make sure that all High Definition Audio components on any particular board configuration are configured in either the 3.3V or 1.5V signaling mode during the board design and are not intermixed together on any platform configuration and in any system state.

6.9 System Timing Budget

The setup and hold numbers at the codec are dependant on the total skew introduced between **BCLK** and **SDO**. This should include signaling induced skews as well as skews due to trace mismatches on the board. Table 13 describes the limits for the total skew allowed on the system. Total skew allowed between BCLK & SYNC and BCLK & RST# is the same as that allowed for **BCLK** & **SDO**, which is described below.

Table 13: Total trace mismatch

Description	Min	Max	Units	Notes
Total skew allowed between BCLK and SDO	-2	2	ns	1

NOTES:

1. This should be the total mismatch in the system including the motherboard and any applicable daughter cards or connectors.

Setup and hold numbers for **SDI** at the controller are dependant on the flight time from the controller to the receiver and vice-versa. Table 14 defines the maximum flight time allowed on the system.

Table 14: Maximum trace lengths

Description	Min	Max	Units	Notes
Flight time for BCLK from controller to the codec	0	7	ns	1
Flight time for SDI from the codec to the controller	0	7	ns	1

NOTES:

1. The maximum flight times in this table will dictate the total maximum allowed trace lengths between the codec

and the controller.

6.10 Physical Requirements

6.10.1 System Board Impedance

This specification was validated using target trace impedance in the range of 55 ohms to 60 ohms with ± 15% allowed tolerance from target. A given system and any add-in cards for that system should pick a target tolerance in this range. The allowed tolerance is then applied to the chosen target impedance.
The system designer has two primary constraints in which to work.

- The length and signal velocity must allow a full round trip time on **BCLK** and **SDI** within the specified round trip propagation delay of 14 ns.

- The loaded impedance seen at any drive point on the network must be such that an High Definition Audio output device (as specified by its V/I curve) can meet input device specifications. This includes loads presented by expansion boards.

6.10.2 Layout Guidelines

Topologies on desktop platforms have been analyzed with microstrip trace models while those on the mobile platforms have been simulated with both stripline and microstrip models. All the trace models used in the simulations to verify this specification were referenced to ground, although that is not a requirement. It is recommended that the reference plane be kept as consistent as possible. Changes in reference plane should have a bypass capacitor between these planes within 0.5 inches.

6.10.3 Trace Length Limits

Suggested trace length limits for each of the branches in the topologies are listed in section 0which describes the different desktop and mobile topologies.

6.11 Topology Configurations

High Definition Audio systems use multi-drop signaling scheme for **BCLK**, **SDO**, **SYNC**, **RST#**. The list of system level topology configurations used to validate this specification (for both 3.3V and 1.5V signaling) has been defined here for reference.

Figure 11 describes the topology configurations that have been simulated on a four layer microstrip desktop platform. Figure 12and Figure 13 describe the topology configurations that have been simulated on a typical multi-layer stripline and microstrip mobile platform. The number of codecs in the system will be limited by the number of SDI pins on the controller.

The intention is to illustrate possible multi-drop topologies. It is expected that system level simulations will be done using the actual trace and board models.

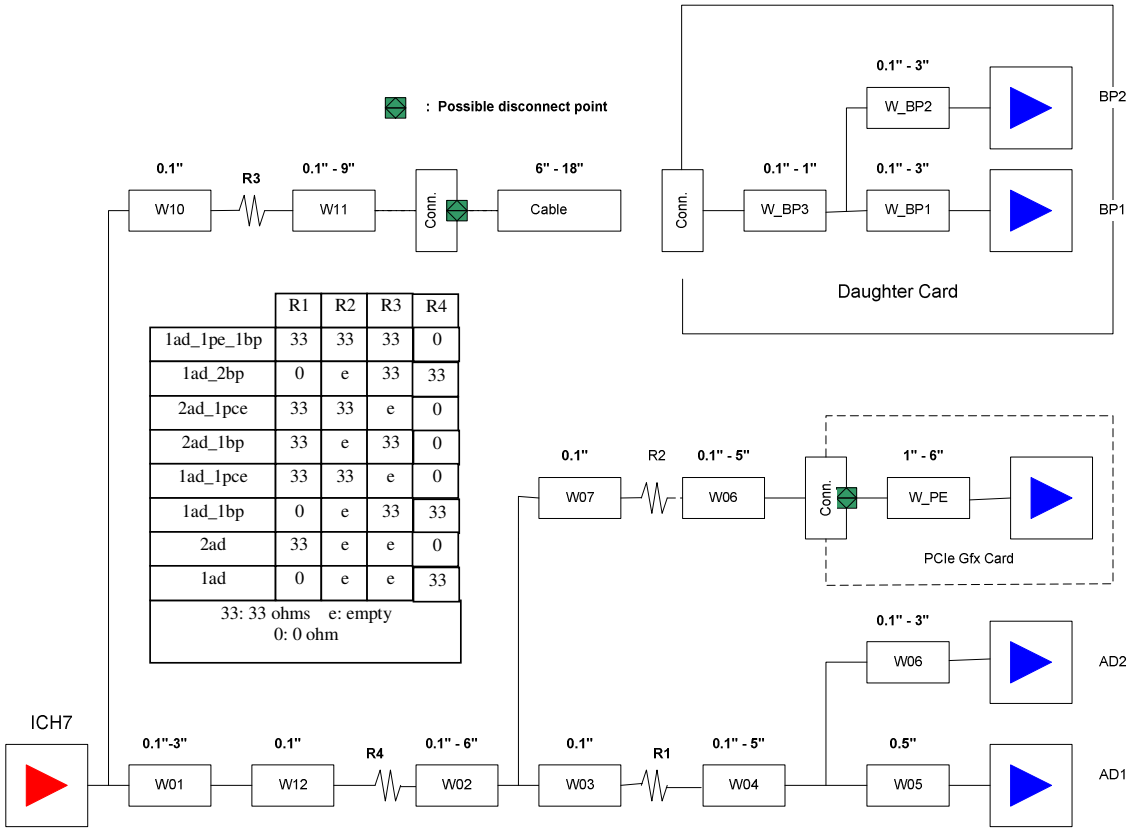

Figure 11: Desktop platform configurations

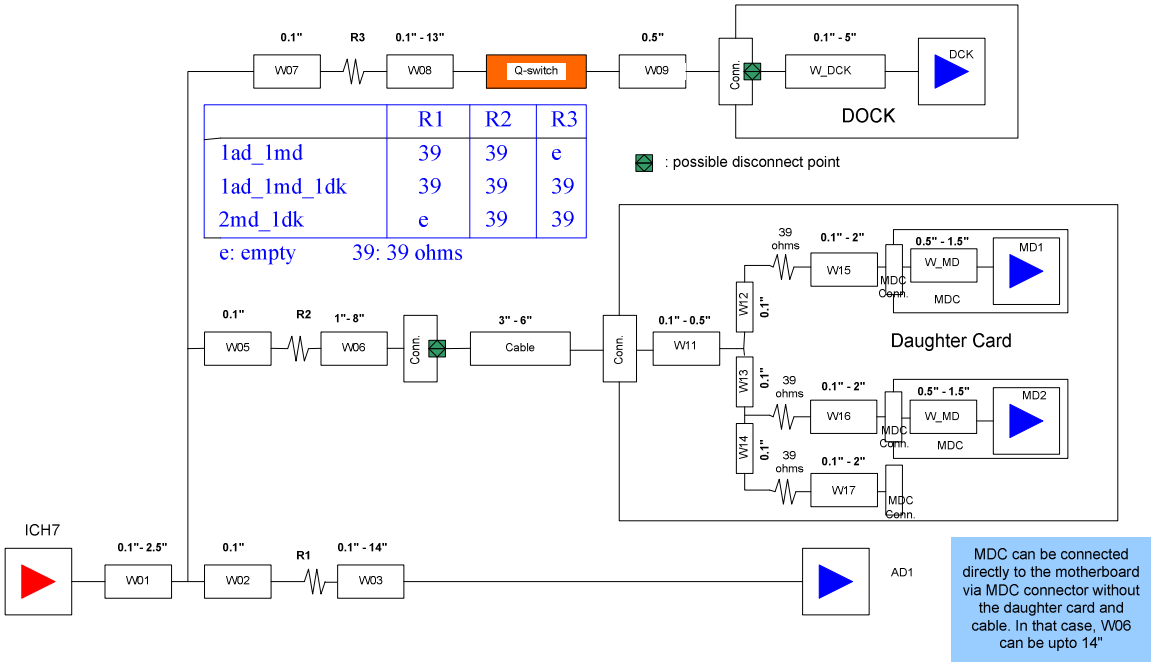

Figure 12: Mobile Star platform configurations

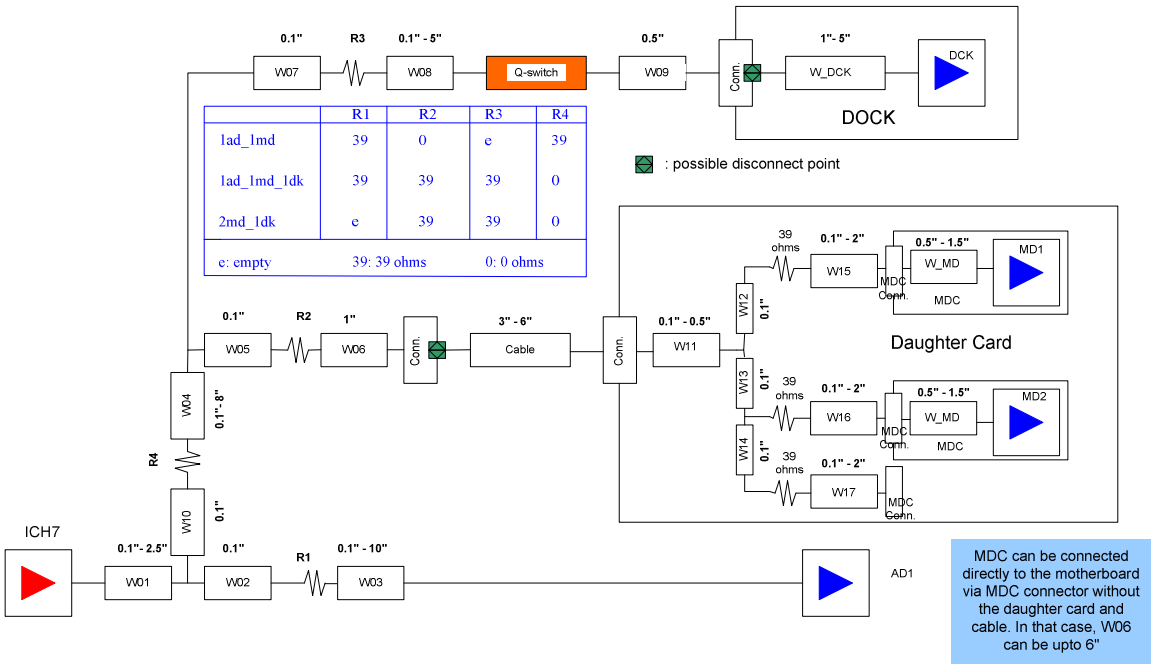

Figure 13: Branched Mobile configuration

6.12 Hot Attach Mechanisms

An important feature for High Definition Audio is supporting hot attach. A typical example is connecting the Codec on the docking station. It is necessary that the part of the link affected by the hot attach is isolated from the remainder of the High Definition Audio link during the connection. This is especially critical on the shared **BCLK**, **SDO**, **SYNC** and **RST#** lines. If this isolation (during hot attach) is ignored, signal quality is highly degraded and would lead to functional failure of the other codecs on the High Definition Audio link.

There are two possible solutions to allow this isolation:

The asynchronous solution, as shown in Figure 14, uses a high speed tri-state buffer as the isolation element during connect. The tri-state buffer is used on the **BCLK**, **SDO**, **SYNC** and **RST#** signals. Since the buffer has a propagation delay, it consumes some of the 14 ns round trip delay allowed for **BCLK** and **SDI**. Consequently, this buffer should be carefully selected to be sure that the total delay meets the round trip flight time requirement. **SDI** is isolated by a simple FET bus switch since there is no shared signals here to be disrupted by the hot attach. The FET switch has a very small propagation delay. The switch prevents having an open line when the line is unconnected.

The synchronous solution to the hot attach problem is shown in Figure 15. This method requires more control logic, but the FET bus switches have much less propagation delay. This makes this scheme more suitable for topologies with longer flight times. The synchronous scheme insures that there is no charge sharing during critical times that will cause glitches on the clock or invalid levels on control or data lines. Such glitches may result in functional failure of the High Definition Audio interface.

Switching of the FET bus switch in this case is made synchronous to the **BCLK** transition; in this case, a positive edge triggered flip flops in the synchronous logic.

As in the case of **BCLK** shown in Figure 15, **SYNC**, **RST#**, **SDO** also has bus switch in the branch that is connected to the hot attach. It is important that the delay through the flip flop to the enabling of the FET bus switch is less than half the clock period to insure that the switch is enabled before the clock falls. This requires careful selection of the flip flops and bus switches for speed. Since DOCK signal turn on is asynchronous to **BCLK**, a minimum of two flip-flops must be used in the enabling scheme, any additional flip-flop stages here would add to the turn on time. Clock charge-sharing problems are be avoided by using a weak pull-up resistor at the DOCK end of the High Definition Audio link. Values of R2 and C1 are selected such that the DOCK codec reset delay is 1ms, given by the equation, R2C1ln [(Vcc - Vthl) / Vcc]. D1 diode used in the reset logic is needed for software initiated reset and should be selected such that the low to high threshold voltage is less than VCC – 700mV.

Any hot attach solution that is defined for High Definition Audio platforms should support both the 3.3V as well as 1.5V signaling. Components used in designing this hot attach schemes should be chosen accordingly so that it meets the system requirements for both 3.3V and 1.5V signaling voltage.

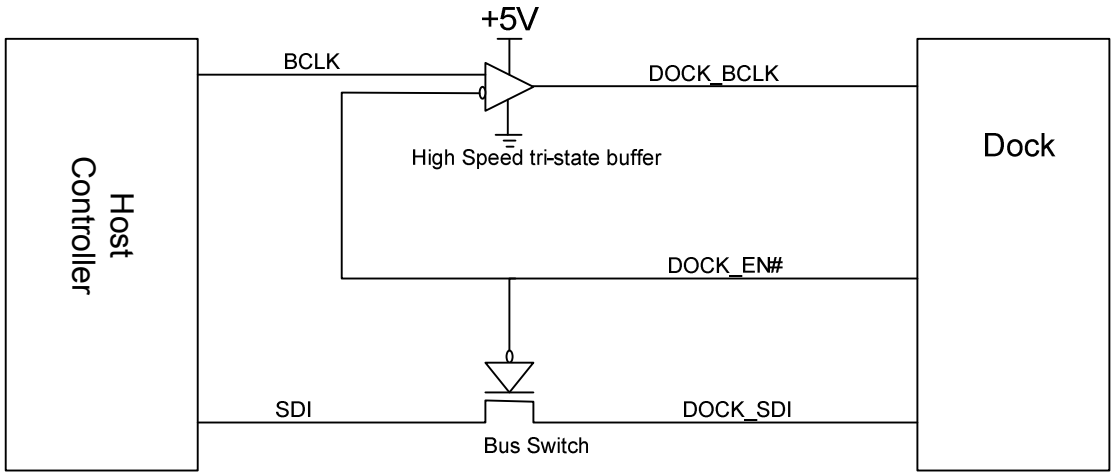

Figure 14: Hot attach Asynchronous solution

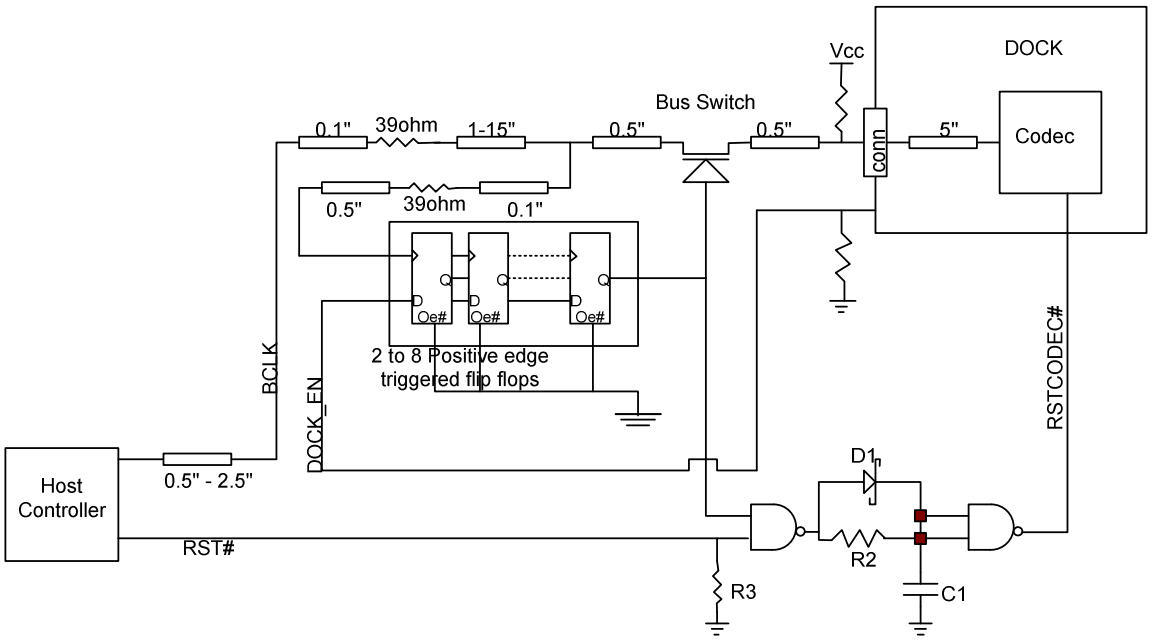

Figure 15: Hot attach, synchronous solution

NOTES:

1. No hot attach solution on AC97 mobile platforms.

An assessment of the impact to the existing revision and systems that currently conform to the HD Audio specification:

No impact known to existing systems. All existing systems will be running at 3.3V signaling.

An analysis of the hardware implications:

No change, except that the High Definition Audio IO supply is separated out from the CORE on the HD Audio components. All components will have the capability to detect the signaling level on the HD Audio IO. The OEM/ODMs must ensure that proper voltages are made available for components that wake the system even though these voltages may not normally be available during lower power states.

An analysis of the software implications:

No impact to the software as change just provides clarity on existing software and hardware implementations.